	Typ	L #	Hits	Search T xt	DBs	Time Stamp
1	BRS	L1	2982	bump near10 (insulat$4 or polyimide or polymer$4)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/11 12:25
3	BRS	L15	388	1 same (stencil$4 or print$4 or stencil-print$4 or stress or stress-buff$6)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/11 12:28
4	BRS	L22	288	15 and (anneal$4 or thermal or cur$4 or heat$4 or temperature)	USPAT; US-PG PUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/11 12:30

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?show files; ds; t/free/all
File   2:INSPEC 1969-2002/Jul W1
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File   3:INSPEC 1969-1982
         (c) 1993 Institution of Electrical Engineers
File   4:INSPEC 1983-2002/Jul W1
         (c) 2002 Institution of Electrical Engineers

Set     Items   Description
S1        104   BUMP (10N) (DIELECTRIC OR INSULAT? OR POLYMER OR POLYIMIDE)
S2         28   S1 AND (STENCIL OR STENCIL-PRINT? OR PRINT?)
S3         12   RD (unique items)
```

3/9/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC
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5430578 INSPEC Abstract Number: B9701-0170J-039
Title: Conductive polymer bump **interconnects**
Author(s): Jong-Kai Lin; Drye, J.; Lytle, W.; Scharr, T.; Subrahmanyan, R.; Sharma, R.
Author Affiliation: Adv. Interconnect Syst. Labs., Motorola Inc., Tempe, AZ, USA
Conference Title: 1996 Proceedings. 46th Electronic Components and Technology Conference (Cat. No.96CH35931) p.1059-68
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 1311 pp.
ISBN: 0 7803 3286 5 Material Identity Number: XX96-01869
U.S. Copyright Clearance Center Code: 0 7803 3286 5/96/$4.00
Conference Title: 1996 Proceedings 46th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 28-31 May 1996 Conference Location: Orlando, FL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T); Experimental (X)
Abstract: Conductive polymer bonded flip chip interconnect systems can provide an attractive alternative flip chip technology in terms of cost and manufacturability. This work examines the feasibility of application of such a technology. A mathematical model for **stencil printing** of conductive adhesive paste is developed to demonstrate some of the factors affecting the **print** quality. Designed experiments is used to optimize **bump** dimensional uniformity. The electrical performance of conductive **polymer** flip chip interconnects is evaluated through both GaAs and Si devices. The microwave insertion loss (S/sub 21/) of a coplanar waveguide test vehicle showed a loss rate of 0.031 dB/GHz for non-underfilled flip chip assembly and 0.065 dB/GHz for those with underfill encapsulation. These S/sub 21/ data are almost identical to a device with same test structure and a Au ball bumped flip chip assembly. Additional test using a CT-2 antenna switch GaAs device flip chip bonded on a FR4 board showed an identical performance (up to 2 GHz frequency) to the same assembly using Au-Sn eutectic bumps. Reliability of conductive polymer bumps was evaluated using Si die flip chip bonded on FR4 substrates. Results showed no failures on temperature cycle, humidity, vibration, and mechanical shock tests. There were 8.6% failures on HAST and 6% failures on thermal shock tests on test conditions stated in the text. (12 Refs)
Subfile: B
Descriptors: conducting materials; conducting polymers; flip-chip devices ; integrated circuit interconnections
Identifiers: conductive **polymer bump** interconnect; HAST; flip chip technology; mathematical model; **stencil printing** ; adhesive paste; electrical performance; GaAs device; Si device; microwave insertion loss; coplanar waveguide; underfill encapsulation; CT-2 antenna switch; Au-Sn eutectic; Au ball; reliability; FR4 substrate; temperature cycling; humidity; vibration; mechanical shock; thermal shock; GaAs; Si; Au-Sn; Au
Class Codes: B0170J (Product packaging)
Chemical Indexing:
GaAs bin - As bin - Ga bin (Elements - 2)
Si el (Elements - 1)
AuSn bin - Au bin - Sn bin (Elements - 2)
Au el (Elements - 1)
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TR 165. P54 V. 1847

3/9/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC
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4432545 INSPEC Abstract Number: B9308-2240-002

Title: Fabrication and assembly processes for solderless flip chip assemblies

Author(s): Estes, R.H.
Author Affiliation: Epoxy Technology, Billerica, MA, USA

Conference Title: ISHM '92 Proceedings. Proceedings of the 1992 International Symposium on Microelectronics (SPIE Vol.1847) p.322-35
Publisher: Int. Soc. Hybrid Microelectron, Reston, VA, USA
Publication Date: 1992 Country of Publication: USA xx+742 pp.
ISBN: 0 930815 35 1
Conference Sponsor: Int. Soc. Hybrid Microelectron
Conference Date: 19-21 Oct. 1992 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P); Experimental (X)

Abstract: A new novel process technology is presented for the manufacture of solderless flip chip assemblies. The technology utilizes high resolution screen **printing** and stencilling of specially formulated dielectric and conductive polymers to form non-metallurgical bumps for flip chip interconnect. Polymer dielectric is deposited onto the surface of a silicon chip, (in wafer form), and cured. The metallized bond pads of the individual chips remain exposed. An electrically conductive, metal filled, **polymer** is then deposited onto the bond pads, in **bump** form, and polymerized. After wafer dicing and test, the 'bumped' flip chips and circuit substrate are aligned and contacted to form the flip chip interconnect. This new **polymer** flip chip process is compared with the traditional 'solder **bump** ' flip chip technology which is currently used in the manufacture of microelectronic assemblies. (15 Refs)

Subfile: B
Descriptors: adhesion; conducting polymers; flip-chip devices; lead bonding; polymer films
Identifiers: polymer dielectric; nonmetallurgical bumps; conductive metal filled polymer; solderless flip chip assemblies; high resolution screen **printing** ; stencilling; conductive polymers; flip chip interconnect; Si chip
Class Codes: B2240 (Microassembly techniques); B0170J (Product packaging)
Chemical Indexing:
Si sur - Si el (Elements - 1)

3/9/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC
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5585729 INSPEC Abstract Number: B9707-0170J-001
Title: Flip-chip packaging with polymer bumps
Author(s): Estes, R.H.
Author Affiliation: Epoxy Technol. Inc., Billerica, MA, USA
Journal: Semiconductor International vol.20, no.2 p.103-4, 106, 108
Publisher: Cahners Publishing,
Publication Date: Feb. 1997 Country of Publication: USA
CODEN: SITLDD ISSN: 0163-3767
SICI: 0163-3767(199702)20:2L.103:FCPW;1-F
Material Identity Number: A681-97003
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: A conductive **polymer bump** process enables a low-temperature flip-chip interconnect technology, requiring only two steps to form conductive bumps on a wafer. Two characteristics of the process-its simplicity and compatibility with fully automated screen and **stencil printers** -are advantageous for high-throughput manufacturing. The lower bonding temperature requirements of the process reduce circuit board assembly and rework costs. (3 Refs)
Subfile: B
Descriptors: adhesion; conducting polymers; flip-chip devices; integrated circuit interconnections; integrated circuit packaging; microassembling
Identifiers: flip-chip packaging; polymer bumps; conductive **polymer bump** process; low-temperature flip-chip interconnect technology; conductive bumps; process compatibility; automated screen **printers** ; automated **stencil printers** ; high-throughput manufacturing; bonding temperature; circuit board assembly cost; rework cost
Class Codes: B0170J (Product packaging); B2240 (Microassembly techniques); B2570 (Semiconductor integrated circuits); B0560 (Polymers and plastics (engineering materials science))
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